WHAT IS CLAIMED IS:

1. A memory device comprising a lamination structure including an insulating film and a semiconductor film, the lamination structure being disposed between an electrode structure and a charge storing node, the lamination structure having an energy band profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing between the electrode structure and the charge storing node in the second configuration.

2. A memory device according to claim 1, wherein the memory device has a control electrode, the energy band profile being changed between the first and the second configuration in response to a voltage supplied to the control electrode.

3. A memory device comprising:

a path for charge carriers;

a charge storing node to produce a field which alters a conductivity of the path; and

a lamination structure including an insulating film and a semiconductor film,

the lamination structure being disposed between an electrode structure and the charge storing node,

the lamination structure having an energy band profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing between the electrode structure and the charge storing node in the second configuration.

4. A memory device according to claim 3, wherein the memory device has a control electrode, the energy band profile being changed between the first configuration and the second configuration in response to a voltage supplied to the control electrode.

5. A memory device comprising:

a source-drain path for charge carriers;

a charge storing node to produce a field which alters a conductivity of the source-drain path; and

a lamination structure including an insulating film and a semiconductor film,

the lamination structure being disposed between electrode structure and the charge storing node,

the lamination structure having an energy band profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing between the electrode structure and the charge storing node in the second configuration.

6. A memory device according to claim 5 wherein the memory device has a control electrode, the energy band profile being changed between the first configuration and the second configuration in response to a voltage supplied to the control electrode.

7. A memory device according to claim 5 wherein the insulating film and the conductive film of the lamination structure are formed of silicon nitride and silicon material, respectively.

8. A memory device according to claim 7 wherein the lamination structure further includes another film of silicon nitride, the silicon material being disposed between the silicon film and the other silicon nitride film.

9. A memory device according to claim 7 wherein the lamination structure further includes another film of silicon material, the silicon nitride film being disposed between the film of silicon material and the other film of silicon material.

10. A memory device according to claim 7 wherein the silicon material comprises polysilicon.

11. A memory device according to claim 8 wherein the silicon material comprises polysilicon.

12. A memory device according to claim 9 wherein the silicon material comprises polysilicon.

13. An electron device comprising a lamination structure including an insulating film and an electrically conductive film, the lamination structure being disposed between a first terminal and a second terminal,

the lamination structure being changeable between a first configuration in which a barrier height of an energy band profile of the lamination structure is high and a second configuration in which a barrier height of an energy band profile of the lamination structure is low, an electric current flowing between the first terminal and the second terminal in the second configuration.

14. An electron device according to claim 13 wherein the memory device has a control electrode, the configurations being changed between the first configuration and the second configuration in response to a voltage applied to the control electrode.

15. A memory device comprising:

a charge storage node,

an electrode structure, and

a barrier structure between the electrode structure and the charge storage node, the barrier structure providing a variable internal electrostatic barrier potential configurable by an external bias to provide selectively a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node, and a relatively high barrier height to store charge carriers on the charge storage node.

16. A memory device according to claim 15 wherein the barrier structure includes a region of barrier material providing a barrier component which is narrower and higher than that provided by the internal electrostatic barrier potential.

17. A memory device according to claim 16 wherein the height of said barrier component is raised and lowered in response to raising and lowering of the height of the barrier provided by the variable internal electrostatic barrier potential.

18. A memory device according to claim 16 wherein the region of barrier material is formed of a material selected from the group consisting of silicon dioxide and silicon nitride.

19. A memory device according to claim 16 including a further said region of barrier material providing a barrier component which is narrower and higher than that provided by the internal electrostatic barrier potential.

20. A memory device according to claim 1 including a gate to receive said external bias to configure the barrier between said high and low barrier heights.

21. A memory device comprising:

a substrate;

an array of memory cells configured on the substrate; and

a plurality of word lines and data lines extending between the cells, the word lines being operable to receive cell selection signals;

each of the memory cells comprising a charge storage node, an electrode forming part of one of the data lines, and a barrier structure between the electrode and the charge storage node, the barrier structure providing a variable internal electrostatic barrier potential configurable selectively in response to an external bias provided by a selection signal applied to one of the word lines to provide a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node, and a relatively high barrier height to store charge carriers on the charge storage node.

22. A memory device according to claim 21 wherein each of the memory cells includes a source-drain path with a conductivity which is altered as a function of the charge stored on the charge storage node, and the device further including a

plurality of sense lines coupled to the source drain paths of the cells, and refreshing circuitry responsive to the sense lines to refresh data on the data lines.

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